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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/885,784	06/20/2001	Mong-Song Liang	67,200-327	3661

7590 10/02/2003

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EXAMINER	
MALDONADO, JULIO J	
ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 10/02/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Advisory Action	Application No.	Applicant(s)	
	09/885,784	LIANG ET AL.	
	Examiner	Art Unit	
	Julio J. Maldonado	2823	

--The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

THE REPLY FILED 07 September 2003 FAILS TO PLACE THIS APPLICATION IN CONDITION FOR ALLOWANCE. Therefore, further action by the applicant is required to avoid abandonment of this application. A proper reply to a final rejection under 37 CFR 1.113 may only be either: (1) a timely filed amendment which places the application in condition for allowance; (2) a timely filed Notice of Appeal (with appeal fee); or (3) a timely filed Request for Continued Examination (RCE) in compliance with 37 CFR 1.114.

PERIOD FOR REPLY [check either a) or b)]

a) ☒ The period for reply expires 3 months from the mailing date of the final rejection.

b) ☐ The period for reply expires on: (1) the mailing date of this Advisory Action, or (2) the date set forth in the final rejection, whichever is later. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of the final rejection.
ONLY CHECK THIS BOX WHEN THE FIRST REPLY WAS FILED WITHIN TWO MONTHS OF THE FINAL REJECTION. See MPEP 706.07(f).

Extensions of time may be obtained under 37 CFR 1.136(a). The date on which the petition under 37 CFR 1.136(a) and the appropriate extension fee have been filed is the date for purposes of determining the period of extension and the corresponding amount of the fee. The appropriate extension fee under 37 CFR 1.17(a) is calculated from: (1) the expiration date of the shortened statutory period for reply originally set in the final Office action; or (2) as set forth in (b) above, if checked. Any reply received by the Office later than three months after the mailing date of the final rejection, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

1. ☐ A Notice of Appeal was filed on _____. Appellant's Brief must be filed within the period set forth in 37 CFR 1.192(a), or any extension thereof (37 CFR 1.191(d)), to avoid dismissal of the appeal.

2. ☐ The proposed amendment(s) will not be entered because:

   (a) ☐ they raise new issues that would require further consideration and/or search (see NOTE below);

   (b) ☐ they raise the issue of new matter (see Note below);

   (c) ☐ they are not deemed to place the application in better form for appeal by materially reducing or simplifying the issues for appeal; and/or

   (d) ☐ they present additional claims without canceling a corresponding number of finally rejected claims.

   NOTE: _____.

3. ☐ Applicant's reply has overcome the following rejection(s): _____.

4. ☐ Newly proposed or amended claim(s) _____ would be allowable if submitted in a separate, timely filed amendment canceling the non-allowable claim(s).

5. ☒ The a)☐ affidavit, b)☐ exhibit, or c)☒ request for reconsideration has been considered but does NOT place the application in condition for allowance because: *See Continuation Sheet*.

6. ☐ The affidavit or exhibit will NOT be considered because it is not directed SOLELY to issues which were newly raised by the Examiner in the final rejection.

7. ☐ For purposes of Appeal, the proposed amendment(s) a)☐ will not be entered or b)☐ will be entered and an explanation of how the new or amended claims would be rejected is provided below or appended.

   The status of the claim(s) is (or will be) as follows:

   Claim(s) allowed: _____.

   Claim(s) objected to: _____.

   Claim(s) rejected: *12,13,16 and 28*.

   Claim(s) withdrawn from consideration: _____.

8. ☐ The proposed drawing correction filed on _____ is a)☐ approved or b)☐ disapproved by the Examiner.

9. ☐ Note the attached Information Disclosure Statement(s)(PTO-1449) Paper No(s). _____.

10. ☐ Other: _____

George Rourson
Primary Examiner

Continuation of 5. does NOT place the application in condition for allowance because: Applicant's arguments filed 09/09/2003 have been fully considered but they are not persuasive.

Applicant argues, "...applicant asserts that Mountain neither explicitly nor implicitly discloses removing a second substrate from a laminated completely fabricated semiconductor integrated circuit microelectronic fabrication while employing a dielectric isolated metallization pattern as a stop layer. Applicant further notes that the Examiner does not apparently assert that Mountain explicitly discloses the same...Thus, Mountain implicitly would have no motivation to employ a dielectric isolated metallization pattern for etch stop purposes, but rather an etch stop layer formed of a single etch stop material appears entirely adequate within Mountain's invention...". In response to these arguments, applicant asserts that Mountain does not expressly teach a laminated completely fabricated semiconductor integrated circuit microelectronic fabrication as claimed. However, Mountain wasn't relied upon that purpose. Mountain was relied on removing substrates and using a dielectric layer as an etch stop layer during such removing step. Furthermore, by including the etch stop layer and the removing steps of Mountain into the laminated completely fabricated semiconductor integrated circuit microelectronic fabrication as taught by Kelly et al., the step of "removing a second substrate from a laminated completely fabricated semiconductor integrated circuit microelectronic fabrication while employing a dielectric isolated metallization pattern as a stop layer" as recited in claim 16 would be achieved.

Also, applicant argues, "...Haq does not apparently require a dielectric isolated metallization pattern by formed upon Haq's substrate prior to thinning thereof, nor does Haq disclose employing the dielectric isolated metallization pattern as a stop layer when thinning Haq's substrate... Haq's invention is preferably employed with the context of a semiconductor substrate having defined on the front side thereo live circuits...Haq's invention is rendered inoperative for its intended purpose since such complete thinning and removal of Haq's semiconductor substrate would also remove Haq's semiconductor devices and render inoperative Haq's live circuits...". In response to this argument, Haq was relied on the teaching of thinning substrates by using CMP processes. Furthermore, Haq teaches that the process may be used on various types of substrate, including live substrates (Haq, column 3, lines 18 - 25)..